Arasan Chip Systems First to Release SD UHS-II PHY IP Core

SAN JOSE, Calif., Aug. 26, 2010 (GLOBE NEWSWIRE) – Arasan Chip Systems, Inc. (“Arasan”), a leading provider of Total Semiconductor IP Solutions, announced that it has developed the UHS-II PHY IP core, a next generation memory interface being finalized by the SD Association. Arasan, an Executive member of the SD Association, has been in deep engagement with its strategic lead customers who are productizing this interface.

The rapid growth of portable media players, megapixel DSC, smartphones, netbooks and gaming consoles has led to the proliferation of non-volatile memory cards to store and distribute HD content. The SD 3.0 specification defines cards with a maximum memory capacity of 2TB and interface bandwidth that scales up to 104MBps in UHS-I.

Anticipating requirements for next generation gaming and multimedia applications, the SD Association has defined a new standard – UHS-II. UHS-II delivers the highest performance non-volatile memory interface, achieving peak interface speeds of 3.12 Gbps in Full duplex mode and 1.56 Gbps in Half duplex mode.

“Implementing the UHS-II interface in an advanced SoC process node requires in-depth understanding of high-speed design and complex mixed-signal interactions,” said Prakash Kamath, Vice President of Engineering at Arasan. “With this release, we are the only company with an end-to-end SD IP solution covering UHS-II controller, PHY and corresponding software stacks.”

With its deep in-house expertise in Mixed Signal design, Arasan has developed a low power, compact, highly integrated UHS-II PHY IP core. The core is available in leading process nodes at multiple foundries. This core can be used in SD host, device as well as other SDIO

configurations. It has been architected to enable easy customer integration and custom porting to any FAB process in a timely manner, to speed up customer time to market.

"To keep pace with the increasing demand for high-performance non-volatile memory interface, Arasan has achieved yet another first – with its high-performance UHS-II PHY IP core," said Somnath Viswanath, Director of Marketing at Arasan. "SoC designers integrating this new standard benefit from our leading edge SD IP cores and Mixed Signal expertise to achieve first silicon success."

Arasan's high-quality UHS-II PHY IP core is designed using our rigorous Mixed Signal design and verification methodology, making Arasan the preferred choice for first time silicon success. Arasan offers a Total IP Solution for this PHY IP core consisting of behavioral model, timing model, GDS II database, LEF model and a LVS netlist. Complementing this core is our complete set of Industry leading SD / SDIO IP controller cores available in multiple configurations.